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AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. **(Currently Amended)** A high efficiency charge pump, comprising:

a first clock signal alternately swinging between a first clock high level and a first clock low level;

a second clock signal alternately swinging between a second clock high level and a second clock low level, in which the second clock high level and the first clock high level are non-overlapping in time with respect to each other;

a first capacitor to which the first clock signal is applied;

a second capacitor to which the second clock signal is applied;

a first former-stage clock signal alternately swinging between a first former-stage clock high level and a first former-stage clock low level;

a second former-stage clock signal alternately swinging between a second former-stage clock high level and a second former-stage clock low level, in which the second former-stage clock high level and the first former-stage clock high level are non-overlapping in time with respect to each other;

a first former-stage capacitor to which the first former-stage clock signal is applied;

a second former-stage capacitor to which the second former-stage clock signal is applied;

a circuit for charging the first former-stage capacitor and the second former-stage capacitor;

a first switching circuit for coupling the second former-stage capacitor with the first capacitor when turned on, such that an amount of charge is transferred between the second former-stage capacitor and the first capacitor;

a second switching circuit for coupling the first former-stage capacitor with the second capacitor when turned on, such that an amount of charge is transferred between the first former-stage capacitor and the second capacitor; and

a first reverse current preventing circuit for turning off the first switching circuit when the first clock signal is at the first clock high level and the second former-stage

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clock signal is at the second former-stage clock low level, thereby preventing a first steady-state reverse current from flowing through the first switching circuit out of the first capacitor, wherein:

a second clock falling edge of the second clock signal from the second clock high level to the second clock low level occurs earlier in time than a second former-stage clock falling edge of the second former-stage clock signal from the second former-stage clock high level to the second former-stage clock low level, and

a second former-stage clock rising edge of the second former-stage clock signal from the second former-stage clock low level to the second former-stage clock high level occurs earlier in time than a second clock rising edge of the second clock signal from the second clock low level to the second clock high level,

thereby turning off the first switching circuit when the second clock signal and the second former-stage clock signal make transitions for preventing a first transition-state reverse current from flowing through the first switching circuit out of the first capacitor.

2. **(Original)** The high efficiency charge pump according to claim 1, wherein:

the first reverse current preventing circuit controls the first switching circuit by using the second former-stage clock signal through the second former-stage capacitor for turning off the first switching circuit when the first clock signal is at the first clock high level and the second former-stage clock signal is at the second former-stage clock low level.

3. **(Original)** The high efficiency charge pump according to claim 1, wherein:

the first reverse current preventing circuit controls the first switching circuit by using the second clock signal through the second capacitor for turning on the first switching circuit when the first clock signal is at the first clock low level and the second clock signal is at the second clock high level.

4. **(Original)** The high efficiency charge pump according to claim 1, wherein:

the first reverse current preventing circuit includes:

a first PMOS transistor controlled by the first clock signal through the first

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capacitor, in which the first PMOS is turned on when the first clock signal is at the first clock low level and the second clock signal is at the second clock high level, such that the second clock signal controls the first switching circuit through the second capacitor, and

a first NMOS transistor controlled by the first clock signal through the first capacitor, in which the first NMOS is turned on when the first clock signal is at the first clock high level and the second former-stage clock signal is at the second former-stage clock low level, such that the second former-stage clock signal controls the first switching circuit through the second former-stage capacitor.

5. **(Original)** The high efficiency charge pump according to claim 1, further comprising:

a second reverse current preventing circuit for turning off the second switching circuit when the second clock signal is at the second clock high level and the first former-stage clock signal is at the first former-stage clock low level, thereby preventing a second steady-state reverse current from flowing through the second switching circuit out of the second capacitor.

6. **(Original)** The high efficiency charge pump according to claim 5, wherein:

the second reverse current preventing circuit controls the second switching circuit by using the first former-stage clock signal through the first former-stage capacitor for turning off the second switching circuit when the second clock signal is at the second clock high level and the first former-stage clock signal is at the first former-stage clock low level.

7. **(Original)** The high efficiency charge pump according to claim 5, wherein:

the second reverse current preventing circuit controls the second switching circuit by using the first clock signal through the first capacitor for turning on the second switching circuit when the second clock signal is at the second clock low level and the first clock signal is at the first clock high level.

8. **(Original)** The high efficiency charge pump according to claim 5, wherein:

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the second reverse current preventing circuit includes:

a second PMOS transistor controlled by the second clock signal through the second capacitor, in which the second PMOS is turned on when the second clock signal is at the second clock low level and the first clock signal is at the first clock high level, such that the first clock signal controls the second switching circuit through the first capacitor, and

a second NMOS transistor controlled by the second clock signal through the second capacitor, in which the second NMOS is turned on when the second clock signal is at the second clock high level and the first former-stage clock signal is at the first former-stage clock low level, such that the first former-stage clock signal controls the second switching circuit through the first former-stage capacitor..

9. (Canceled)

10. **(Original)** The high efficiency charge pump according to claim 1, wherein:

a first clock falling edge of the first clock signal from the first clock high level to the first clock low level occurs earlier in time than a first former-stage clock falling edge of the first former-stage clock signal from the first former-stage clock high level to the first former-stage clock low level, and

a first former-stage clock rising edge of the first former-stage clock signal from the first former-stage clock low level to the first former-stage clock high level occurs earlier in time than a first clock rising edge of the first clock signal from the first clock low level to the first clock high level,

thereby turning off the second switching circuit when the first clock signal and the first former-stage clock signal make transitions for preventing a second transition-state reverse current from flowing through the second switching circuit out of the second capacitor.

11. **(Currently Amended)** A high efficiency charge pump, comprising:

a first clock signal alternately swinging between a first clock high level and a first clock low level;

a second clock signal alternately swinging between a second clock high level and

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a second clock low level, in which the second clock high level and the first clock high level are non-overlapping in time with respect to each other;

a first capacitor to which the first clock signal is applied;

a second capacitor to which the second clock signal is applied;

a first former-stage clock signal alternately swinging between a first former-stage clock high level and a first former-stage clock low level;

a second former-stage clock signal alternately swinging between a second former-stage clock high level and a second former-stage clock low level, in which the second former-stage clock high level and the first former-stage clock high level are non-overlapping in time with respect to each other;

a first former-stage capacitor to which the first former-stage clock signal is applied;

a second former-stage capacitor to which the second former-stage clock signal is applied;

a circuit for charging the first former-stage capacitor and the second former-stage capacitor;

a first switching circuit for coupling the second former-stage capacitor with the first capacitor when turned on, such that an amount of charge is transferred between the second former-stage capacitor and the first capacitor; and

a second switching circuit for coupling the first former-stage capacitor with the second capacitor when turned on, such that an amount of charge is transferred between the first former-stage capacitor and the second capacitor, wherein:

a second clock falling edge of the second clock signal from the second clock high level to the second clock low level occurs earlier in time than a second former-stage clock falling edge of the second former-stage clock signal from the second former-stage clock high level to the second former-stage clock low level, and

a second former-stage clock rising edge of the second former-stage clock signal from the second former-stage clock low level to the second former-stage clock high level occurs earlier in time than a second clock rising edge of the second clock signal from the second clock low level to the second clock high level,

thereby turning off the first switching circuit when the second clock signal and the second former-stage clock signal make transitions for preventing a first

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transition-state reverse current from flowing through the first switching circuit out of the first capacitor.

12. **(Original)** The high efficiency charge pump according to claim 11, wherein:

a first clock falling edge of the first clock signal from the first clock high level to the first clock low level occurs earlier in time than a first former-stage clock falling edge of the first former-stage clock signal from the first former-stage clock high level to the first former-stage clock low level, and

a first former-stage clock rising edge of the first former-stage clock signal from the first former-stage clock low level to the first former-stage clock high level occurs earlier in time than a first clock rising edge of the first clock signal from the first clock low level to the first clock high level,

thereby turning off the second switching circuit when the first clock signal and the first former-stage clock signal make transitions for preventing a second transition-state reverse current from flowing through the second switching circuit out of the second capacitor.

13. **(Original)** The high efficiency charge pump according to claim 11, wherein:

the first switching circuit is controlled by the second clock signal through the second capacitor, and

the second switching circuit is controlled by the first clock signal through the first capacitor.

14. **(Original)** The high efficiency charge pump according to claim 11, wherein:

the first clock high level is equal to the second clock high level;

the first clock low level is equal to the second clock low level;

the first former-stage clock high level is equal to the second former-stage clock high level; and

the first former-stage clock low level is equal to the second former-stage clock low level.

15. **(Original)** The high efficiency charge pump according to claim 11, wherein:

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the first switching circuit is an NMOS transistor having a control electrode coupled to the second capacitor, a first current electrode coupled to the second former-stage capacitor, and a second current electrode coupled to the first capacitor.

16. **(Original)** The high efficiency charge pump according to claim 11, wherein:

the second switching circuit is an NMOS transistor having a control electrode coupled to the first capacitor, a first current electrode coupled to the first former-stage capacitor, and a second current electrode coupled to the second capacitor.

17. **(Currently Amended)** A method of converting a voltage with high efficiency, comprising steps of:

applying to a first capacitor a first clock signal alternately swinging between a first clock high level and a first clock low level;

applying to a second capacitor a second clock signal alternately swinging between a second clock high level and a second clock low level, in which the second clock high level and the first clock high level are non-overlapping in time with respect to each other;

applying to a first former-stage capacitor a first former-stage clock signal alternately swinging between a first former-stage clock high level and a first former-stage clock low level;

applying to a second former-stage capacitor a second former-stage clock signal alternately swinging between a second former-stage clock high level and a second former-stage clock low level, in which the second former-stage clock high level and the first former-stage clock high level are non-overlapping in time with respect to each other;

coupling a first current electrode of a first switching circuit with the second former-stage capacitor and coupling a second current electrode of the first switching circuit with the first capacitor;

coupling a first current electrode of a second switching circuit with the first former-stage capacitor and coupling a second current electrode of the second switching circuit with the second capacitor;

charging the first former-stage capacitor and the second former-stage capacitor;

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coupling a control electrode of the first switching circuit with the second current electrode of the second switching circuit when the first clock signal is at the first clock low level and the second clock signal is at the second clock high level; and

coupling the control electrode of the first switching circuit with the first current electrode of the first switching circuit when the first clock signal is at the first clock high level and the second former-stage clock signal is at the second former-stage clock low level., wherein:

a second clock falling edge of the second clock signal from the second clock high level to the second clock low level occurs earlier in time than a second former-stage clock falling edge of the second former-stage clock signal from the second former-stage clock high level to the second former-stage clock low level, and

a second former-stage clock rising edge of the second former-stage clock signal from the second former-stage clock low level to the second former-stage clock high level occurs earlier in time than a second clock rising edge of the second clock signal from the second clock low level to the second clock high level.

18. **(Original)** The method according to claim 17, further comprising steps of:

coupling a control electrode of the second switching circuit with the second current electrode of the first switching circuit when the second clock signal is at the second clock low level and the first clock signal is at the first clock high level, and

coupling the control electrode of the second switching circuit with the first current electrode of the second switching circuit when the second clock signal is at the second clock high level and the first former-stage clock signal is at the first former-stage clock low level.

19. **(Canceled)**

20. **(Original)** The method according to claim 17, wherein:

a first clock falling edge of the first clock signal from the first clock high level to the first clock low level occurs earlier in time than a first former-stage clock falling edge of the first former-stage clock signal from the first former-stage clock high level to the first former-stage clock low level, and

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a first former-stage clock rising edge of the first former-stage clock signal from the first former-stage clock low level to the first former-stage clock high level occurs earlier in time than a first clock rising edge of the first clock signal from the first clock low level to the first clock high level.

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